**Simulation results.**

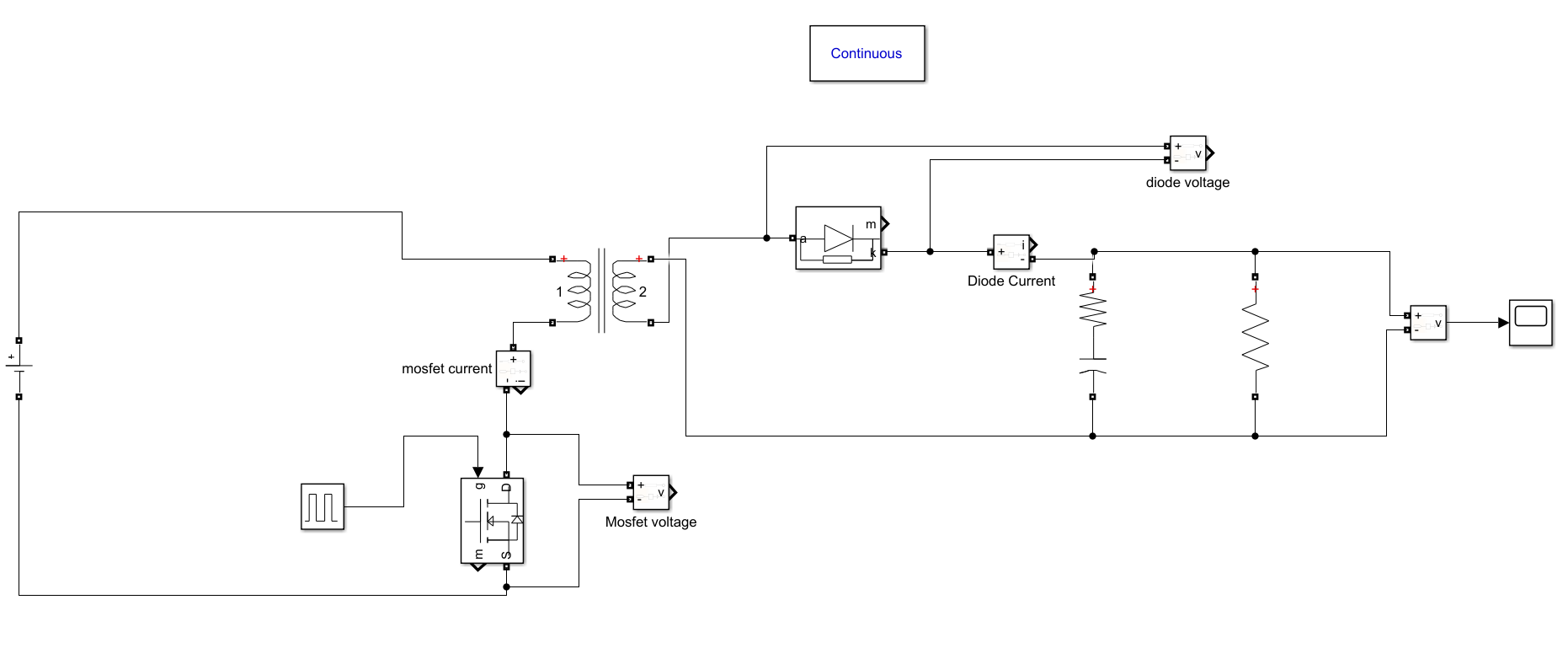
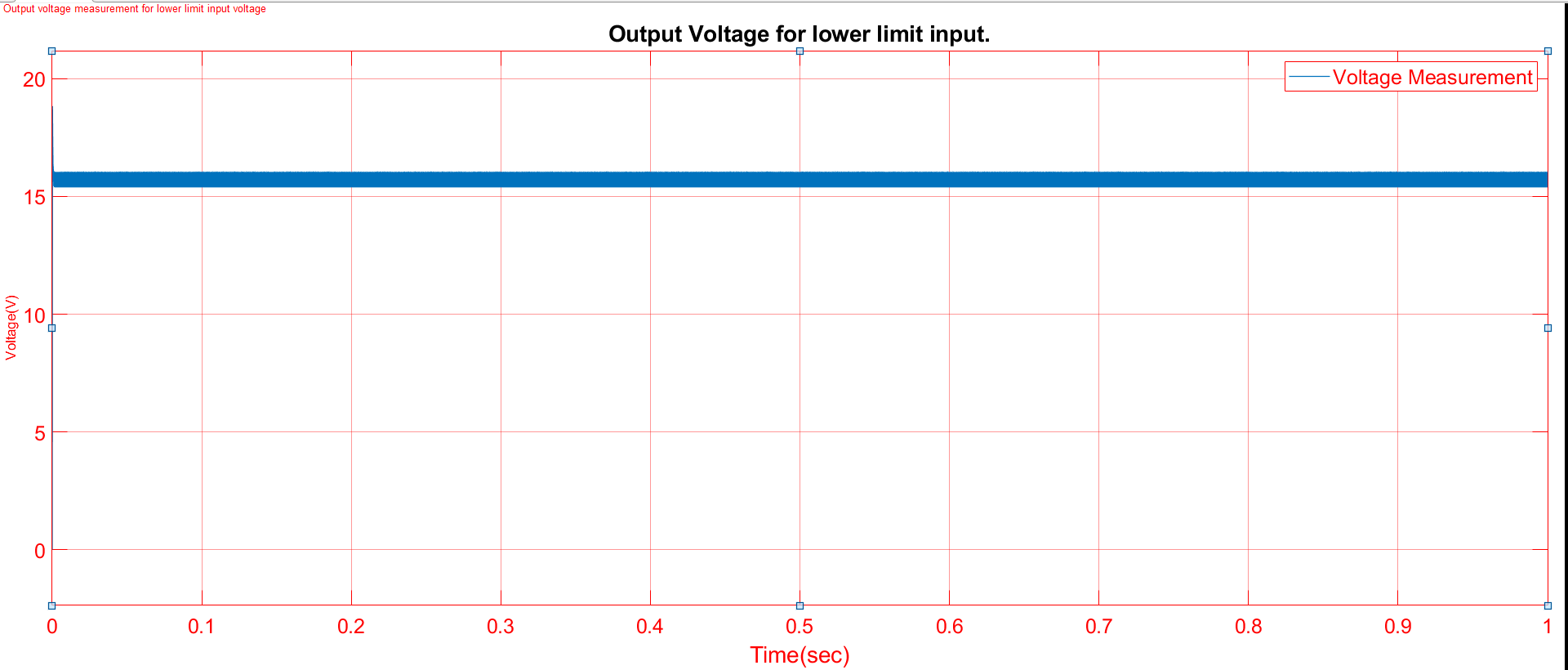
****

Figure xX: Circuit diagram of the project.

1. **Output voltage verification.**

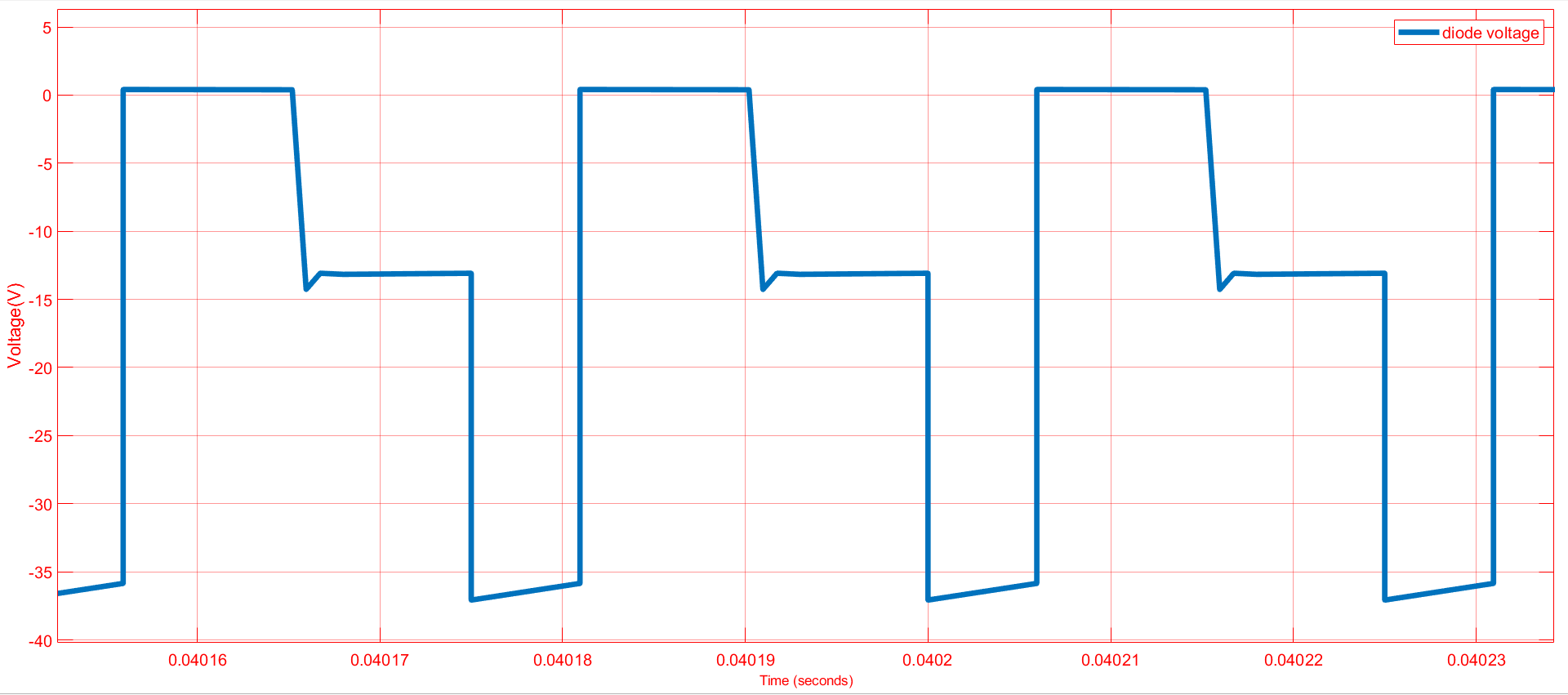
In order to observer how much the duty cycle is deviated from the ideal case to compansate non linearities.

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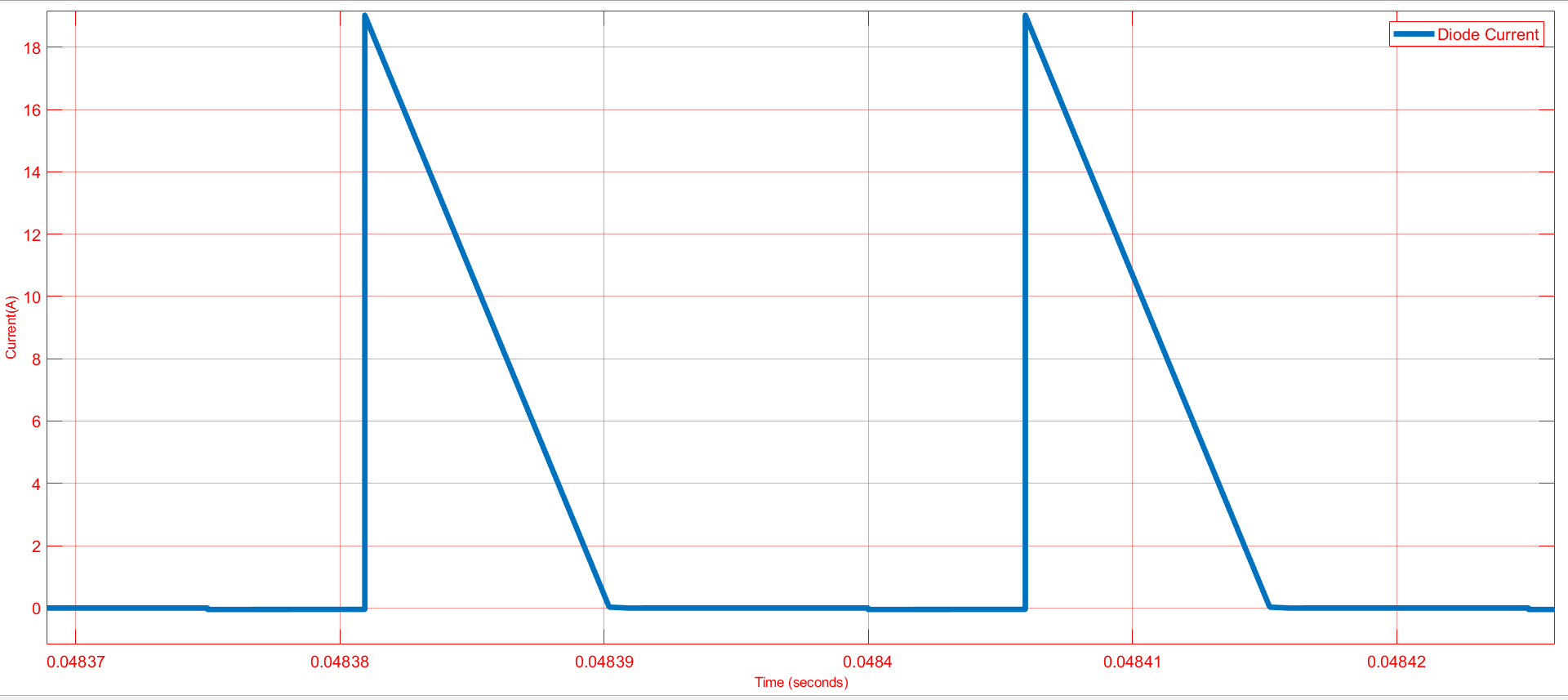
FigureXX: Output voltage verification.

1. **Diode ratings**

* This simulation is done such that the duty cycle is the value that creates most voltage stress on the diode and also highest current.

****

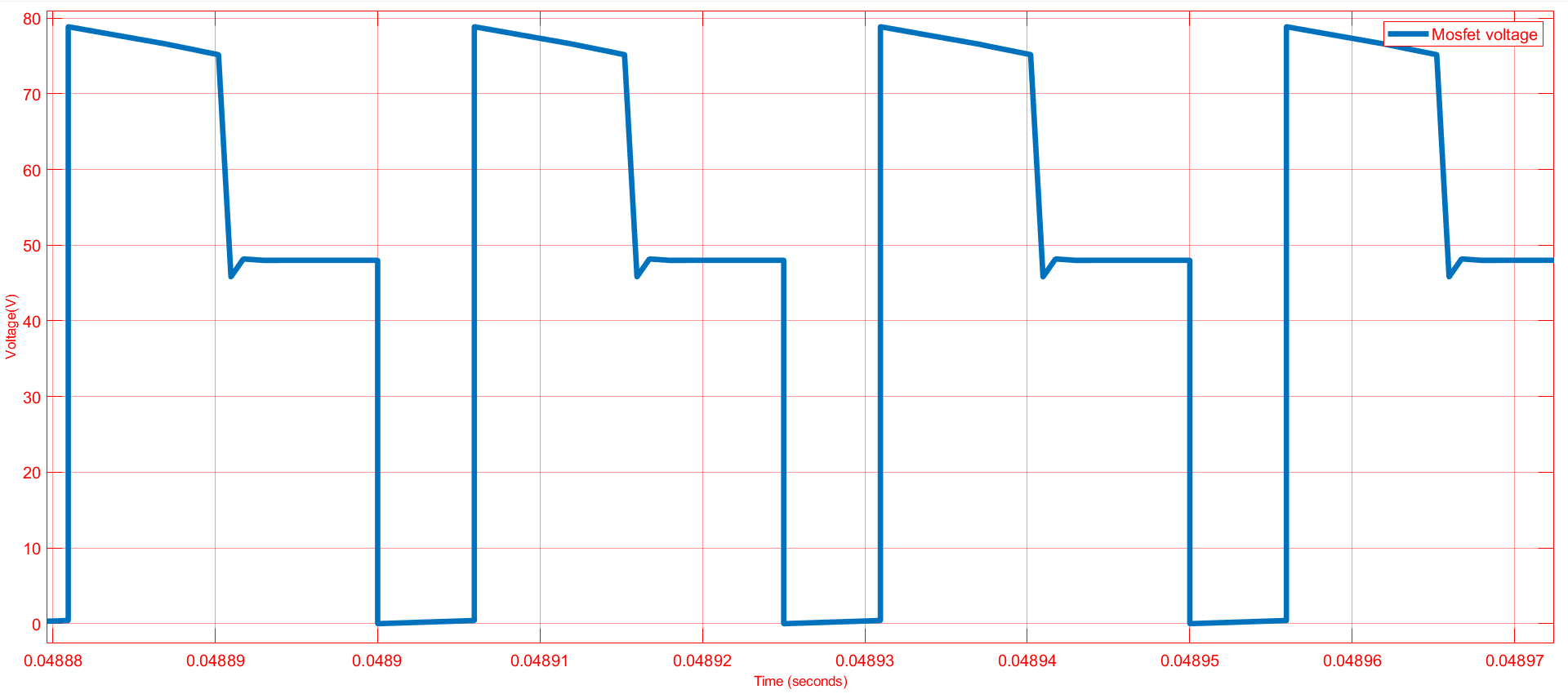
FigureXX: Voltage stress on the diode.

****

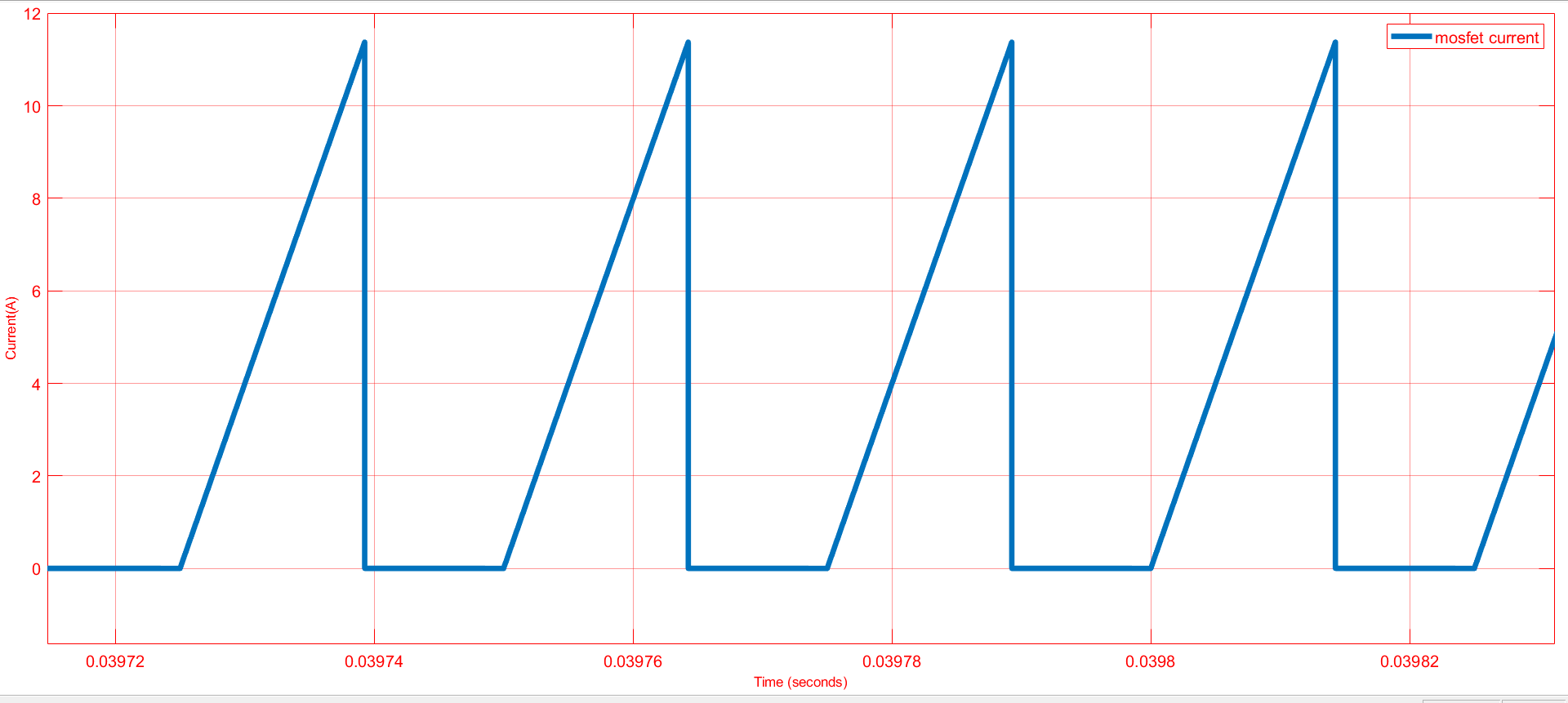
FigureXX: Current stress on the diode.

1. **Mosfet ratings.**

* This simulation has been done under the conditions where the mosfet current and voltage at its highest value.

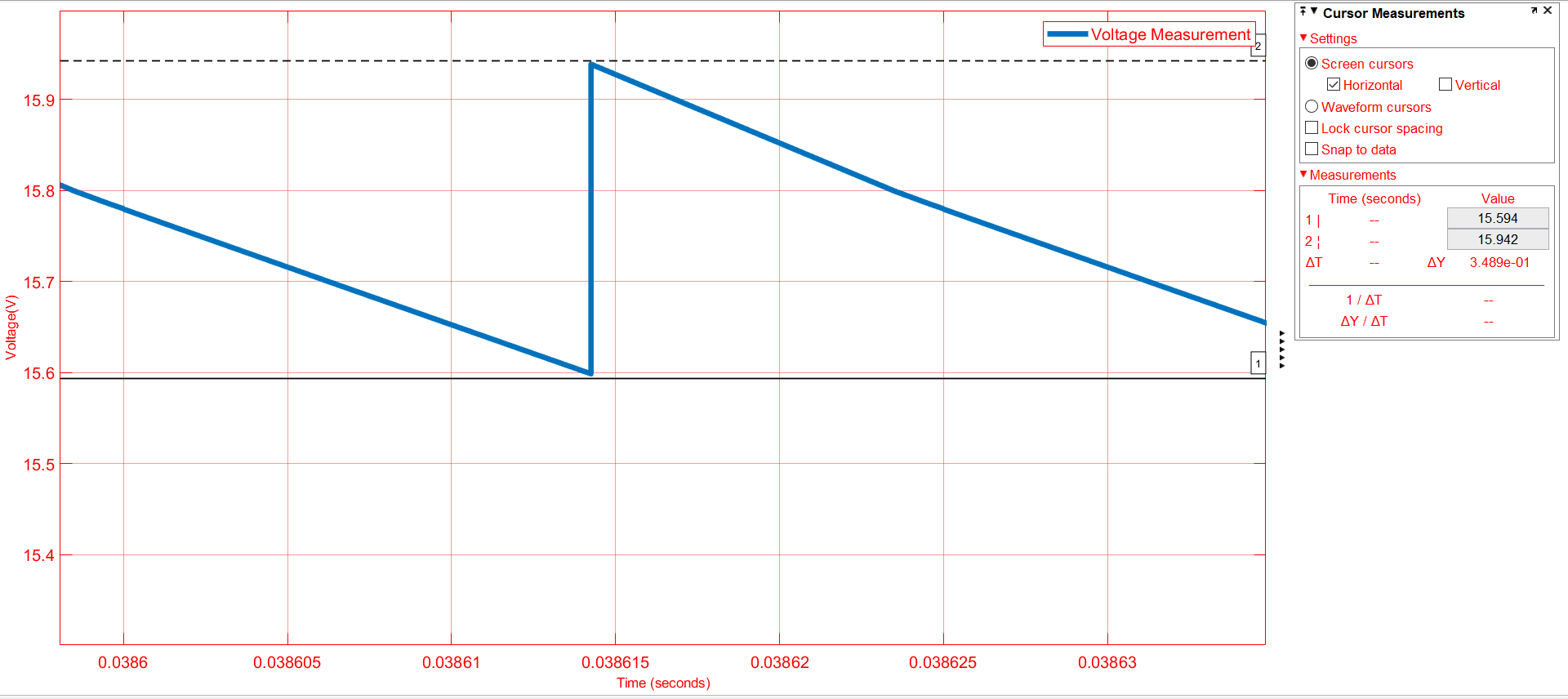
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FigureXX: Voltage stress on the mosfet.

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FigureXX:Current stress on the mosfet.

1. **Output ripple.**

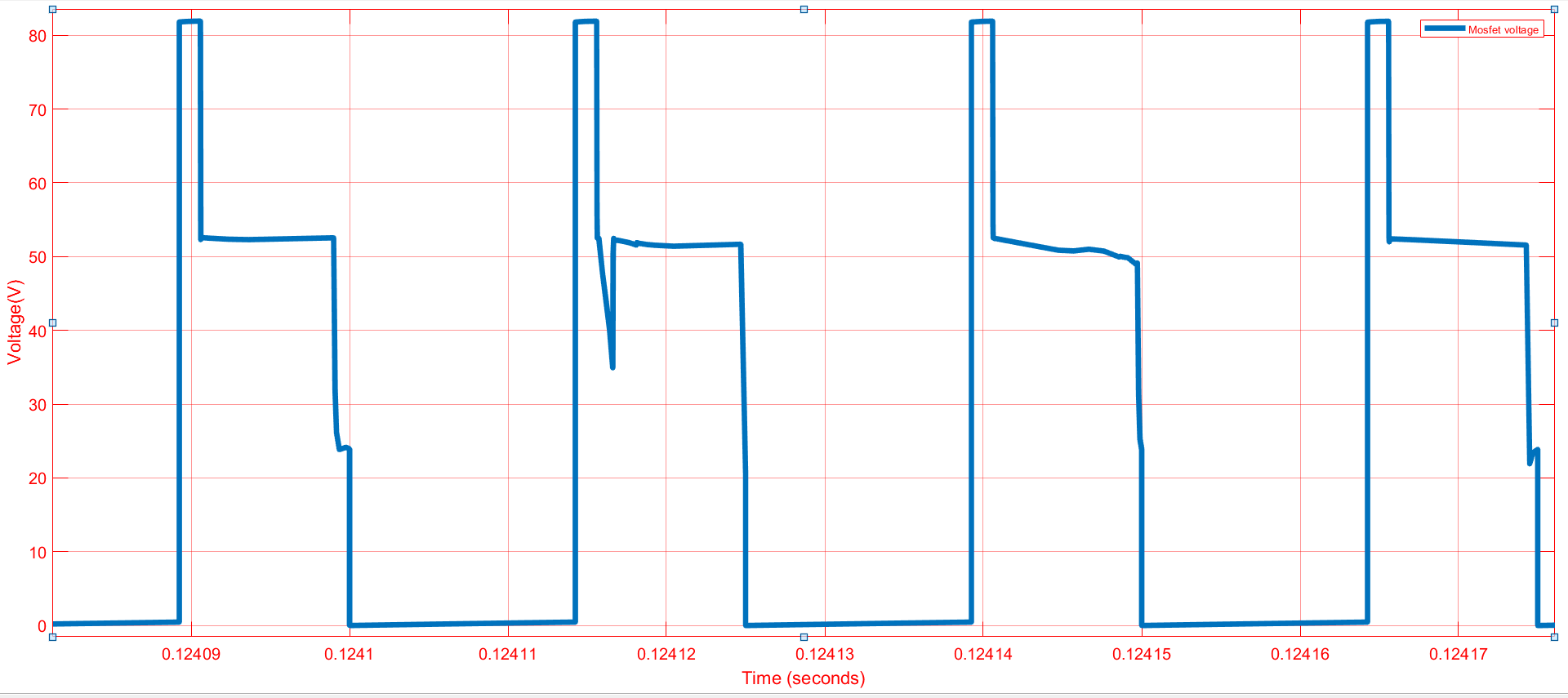
****

FigureXX: Output ripple.

* Output voltage ripple is approximately %2.5 according to the simulation result.

1. **Snubber**

* Snubber is designed not to exceed our mosfet voltage limit and also providing enough time to dissipate the energy on the leakage inductances.

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FigureXX: Voltage stress on the mosfet with snubber.